Am9513
SYSTEM TIMING CONTROLLER DETAILED FUNCTIONAL DESCRIPTION

ADVANCED MICRO DEVICES

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INTRODUCTION

General

Manipulation and coordination of timing parameters and event sequences are universal system attributes. At the most fundamental levels of control, time sequences are intimately embedded in the essential hardware and interface concepts of all processors: the necessary flows of step-by-step procedures are inherent in the execution of even the most basic programs. At the interface level, both internal and external hardware coordination usually require several types of timing-oriented exchanges. In general, control of system and sub-system processes will often involve sophisticated levels of counting, sequencing and timing manipulations. The specific mix of such activities will, of course, be application dependent, yet counting/timing concepts are at least fundamentally involved in all system operations, from the simplest sequencing of a hardware interface to the complex interaction of high-level processes.

Time-related activities fall into a wide variety of categories. Frequency generation, waveform duty cycle control, event counting, interval measurement, precise periodic interrupts, time-of-day accumulation, delays, gap detection, etc., are just a few of the types of operations typically undertaken. When the system must accomplish several of these activities, especially when some measure of concurrency is necessary, a significant portion of the available processing and/or hardware logic resources can be consumed. Throughput limitations easily arise.

A specialized circuit with enough versatility to handle many types of counting and timing functions would therefore be able to simplify software, improve system performance and decrease system chip count. The Am9513 System Timing Controller has been designed to accomplish just such a task. It provides significant capability for waveform generation, counting, timing and intervalometer functions for many types of processor-oriented systems. It offers an unusually versatile control structure that allows the use of many operating configurations so that a wide variety of applications can be efficiently serviced.

The operating philosophy of the Am9513 is based on the use of general-purpose counters that can be controlled in various ways to produce the functions desired. Broadly, use of the counters falls into two classic categories: (a) count accumulation, and (b) frequency division.

In the first case, the counter simply accumulates a count of transitions that occur on its input. An output that indicates the zero state of the counter would be of only incidental interest. The counter value should be available at any time to the associated CPU or it might be compared with some independent value. The accumulated count might be modified or the counter input conditioned by various controls, including hardware and software gating functions; in any event, in these types of applications, it is the value of the actual count that is of interest.

In the case of frequency division, on the other hand, it is an output waveform that is of interest and the counter input information may be incidental. With an output signal that indicates the zero state of the counter, selection of the effective length of the counter and the input frequency are controlled to provide the desired output frequency. Additional controls may allow various types of output waveforms to be generated from the base output frequency, but the actual counter value will usually not be of direct interest.

The Am9513 has been designed to handle effectively both modes of operation, even intermixed on the same chip. In many instances, of course, both types of counter usage will be combined to provide the desired function.

Feature Overview

The Am9513 System Timing Controller (STC) is a support device for processor oriented systems that is designed to enhance the available capability with respect to counting and timing operations. A single Am9513 contains an internal oscillator and associated frequency scaling circuitry plus five general-purpose 16-bit counters. Each counter is supported by control circuitry that allows it to be independently configured for a variety of tasks. The data bus interface to the host processor may be either 8 bits or 16 bits wide.

The internal frequency source is designed for use with an external frequency-determining crystal or other reactive network. The output of the oscillator is scaled so that five different internal frequencies are available for selection as inputs for each of the counters. Any of the internal frequencies may also be brought out for use in other parts of the system.

Each counter can be programmed to count up or count down and to count in binary or in BCD. There are 16 counting sources available for each counter and input polarity is also individually selectable. Gating functions allow direct hardware and software control of the count accumulation. Several combinations of output configurations and polarities are available. Modulo control of the counters is provided by allowing automatic initialization of the counter from a control register when the count reaches zero. Any of the counters may be internally concatenated with an adjacent one in order to form a larger count capability.

Counters 1 and 2, in addition to their usage like the other counters, may also be configured to operate in a time-of-day mode providing a 24-hour real-time clock. Auxiliary alarm registers on counters 1 and 2 may be used to compare the counter contents with previously entered values.

The many internal control and operating elements of the STC may be accessed by the host processor in several ways. Random access to any element for either reading or writing is easily accomplished using an addressing command before each data transfer. Alternatively, automatic sequential access can be used without command intervention, and will simplify many operating procedures.

The Am9513 is implemented in a scaled N-channel silicon gate MOS technology with drawn gates as small as 4 microns. This process features low profile structures with both depletion and enhancement transistors, and results in very small, low capacitance, low-power, high-speed circuitry. The chip contains more than 13,000 transistors within a total chip area of less than 34,200 square mils.

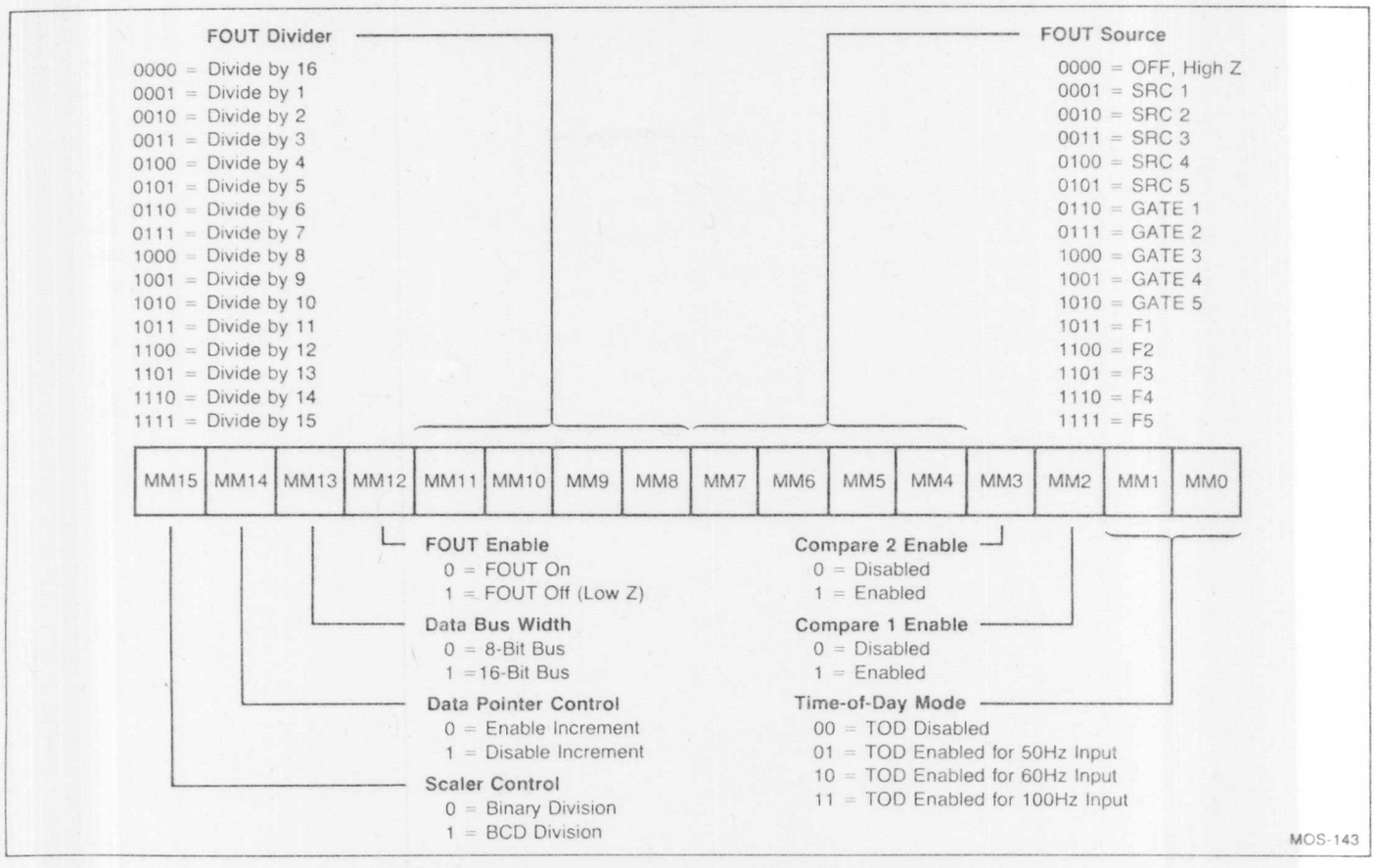


Figure 6. Master Mode Register Bit Assignments.

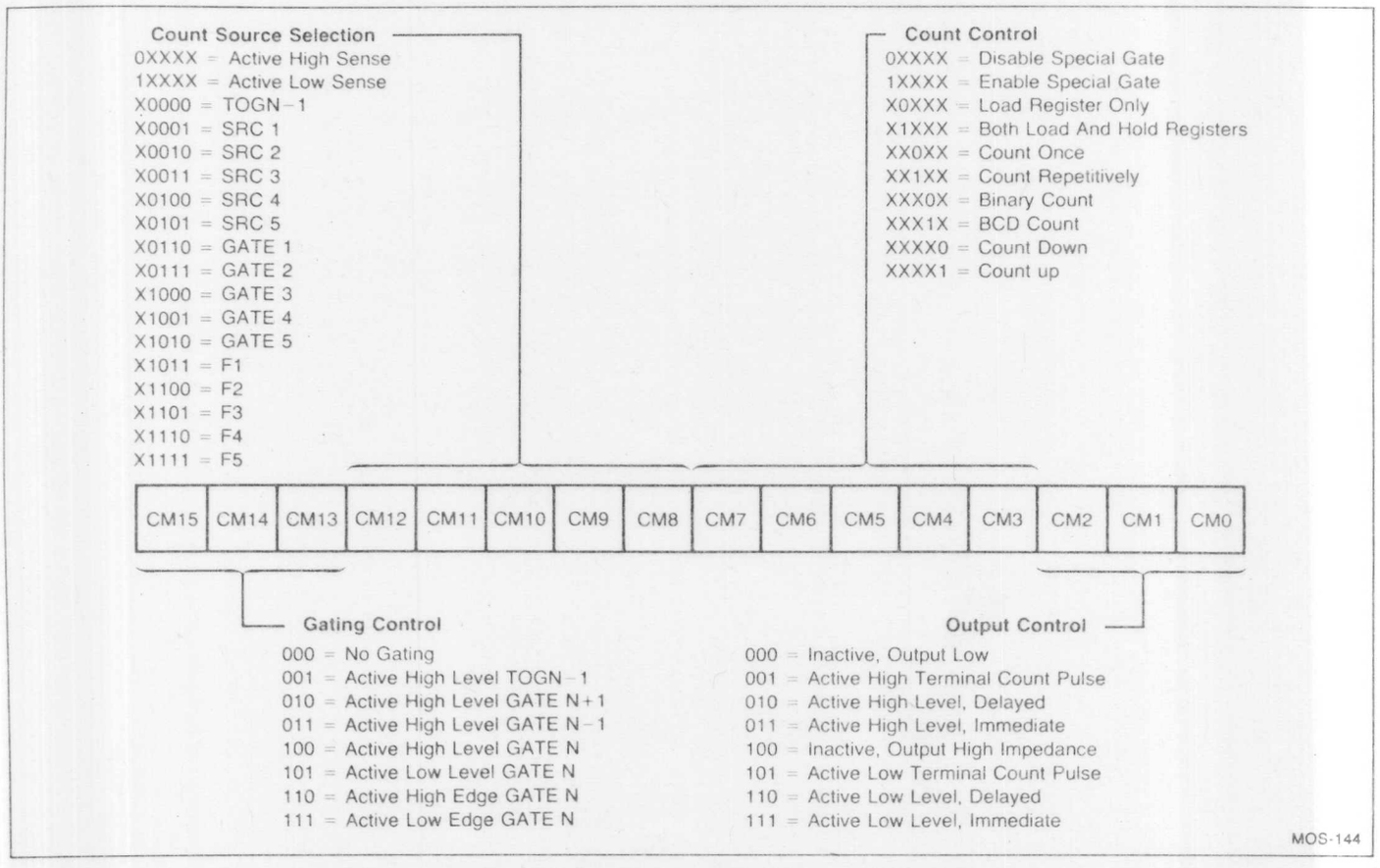


Figure 7. Counter Mode Register Bit Assignments.

Any of three different GATE pins may be specified for level-sensitive gating. The toggle output from the adjacent counter can also be used as a gate source.

Command Summary

Figure 8 lists the command codes for the Am9513. Commands are entered by writing into the control port. The six types of commands that use the linear-select five-bit S field are designed to allow any individual counter or any combination of counters to be operated upon by a single command. Software routines may then be counter-specific without interfering with other count processes that may be under way, yet multiple counters can be simultaneously controlled when desired. The S1 bit designates Counter 1, S2 is Counter 2, etc.

Other commands allow direct control of some of the important Master Mode control bits as an alternative to parallel loading of all bits of the MM register. The data pointer register is used to address the internal element to be operated on by a succeeding data read or write operation. A command is used to load the pointer and thus to allow random access to any of the internal locations. (The data pointer may also be automatically sequenced.) Software stepping of an individual counter is available via command.

Command Code								Command Description
C7	C6	C5	C4	C3	C2	C1	C0	
0	0	0	0	0	0	0	0	No operation
0	0	0	E2	E1	G4	G2	G0	Load Data Pointer register with contents of E and G fields. $G \neq 000$, $G \neq 110$
0	0	1	S1	S2	S3	S4	S5	Arm counting for all selected counters
0	1	0	S1	S2	S3	S4	S5	Load all selected counters
0	1	1	S1	S2	S3	S4	S5	Load and Arm all selected counters
1	0	0	S1	S2	S3	S4	S5	Disarm and Save all selected counters
1	0	1	S1	S2	S3	S4	S5	Save all selected counters
1	1	0	S1	S2	S3	S4	S5	Disarm all selected counters
1	1	1	0	0	N4	N2	N1	Set output bit N ($001 \leq N \leq 101$)
1	1	1	0	1	N4	N2	N1	Clear output bit N ($001 \leq N \leq 101$)
1	1	1	1	0	N4	N2	N1	Step counter N ($001 \leq N \leq 101$)
1	1	1	0	0	0	0	0	Set MM14 (Disable access increment)
1	1	1	0	0	1	1	0	Set MM12 (Disable FOUT)
1	1	1	0	0	1	1	1	Set MM13 (Enter 16-bit bus mode)
1	1	1	0	1	0	0	0	Clear MM14 (Enable access increment)
1	1	1	0	1	1	1	0	Clear MM12 (Enable FOUT)
1	1	1	0	1	1	1	1	Clear MM13 (Enter 8-bit bus mode)
1	1	1	1	1	1	1	1	Master reset

Figure 8. Am9513 Command Summary.

SRC1-SRC5 (Source, Inputs)

The Source inputs provide external signals that may be counted by any of the counters. Any Source line may be routed to any or all of the counters and the FOUT divider. The active polarity for a selected SRC input is programmed at each counter. Any duty cycle waveform will be accepted as long as the minimum pulse width is at least half the period of the maximum specified counting frequency for the part. Schmitt-trigger circuitry on the SRC inputs allows slow transition times to be used.

OUT1-OUT5 (Counter Outputs)

Each three-state OUT signal is directly associated with a corresponding individual counter. Depending on the counter configuration, the OUT signal may be a pulse, a square wave, or a complex duty cycle waveform. OUT polarities are individually programmable. The output circuitry detects the counter state that would have been all bits zero in the absence of a reinitialization. That information is used to generate the selected waveform type.

DB0-DB7, DB8-DB15 (Data Bus, Input/Output)

The Data Bus lines are used for information exchanges with the host processor. After power-up or reset, the data bus will be configured for 8-bit width and will use only DB0 through DB7. It may be reconfigured for 16-bit width by changing a control bit in the Master Mode register. This is accomplished by writing an 8-bit command into the low-order DB lines while holding the high-order lines at a logic high level. Thereafter all 16 lines can be used.

When operating in the 8-bit data bus environment, DB8 through DB12 may optionally be used as additional Gate inputs. See Figure 6. If unused they should be held high. When pulled low, a GateNA signal will disable the action of the corresponding counter N gating. DB13-15 should be held high.

Package Pin	Data Bus Width (MM14)	
	16 Bits	8 Bits
12	DB0	DB0
13	DB1	DB1
14	DB2	DB2
15	DB3	DB3
16	DB4	DB4
17	DB5	DB5
18	DB6	DB6
19	DB7	DB7
20	DB8	GATE 1A
22	DB9	GATE 2A
23	DB10	GATE 3A
24	DB11	GATE 4A
25	DB12	GATE 5A
26	DB13	(VIH)
27	DB14	(VIH)
28	DB15	(VIH)

Figure 6. Data Bus Assignments.

$\overline{CS}$ (Chip Select, Input)

The active-low Chip Select input enables Read and Write operations on the data bus. When Chip Select is high, the Read and Write inputs are ignored. The first Chip Select signal after power-up is used to clear the power-on-reset circuitry.

$\overline{RD}$ (Read, Input)

The active-low Read signal is conditioned by Chip Select and indicates that internal information is to be transferred to the data bus. The source will be determined by the port being addressed and by the Data Pointer register. $\overline{WR}$ and $\overline{RD}$ should be mutually exclusive.

$\overline{WR}$ (Write, Input)

The active-low Write signal is conditioned by Chip Select and indicates that data bus information is to be transferred to an internal location. The destination will be determined by the port being addressed and by the Data Pointer register. $\overline{WR}$ and $\overline{RD}$ should be mutually exclusive.

C/$\overline{D}$ (Control/Data, Input)

The Control/Data signal selects the port used for Read and Write transfers. Control Write operations load the command register and Control Read operations output the status register. Data Read and Data Write operations are made with all other internal registers. See Figure 7. Indirect addressing at the data port is controlled internally by the Data Pointer register.

Signal Configuration				Data Bus Operation
$\overline{CS}$	C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	
0	0	0	1	Transfer contents of data register addressed by Data Pointer to data bus.
0	0	1	0	Transfer contents of data bus to data register addressed by Data Pointer.
0	1	0	1	Transfer contents of Status register to data bus.
0	1	1	0	Transfer contents of data bus into Command register.
X	X	1	1	No transfer.
1	X	X	X	No transfer.

Figure 7. Data Bus Transfers.

Interface Considerations

All of the input and output signals for the Am9513 are specified with logic levels identical to those of standard TTL circuits. The worst-case input logic levels are 2.0V high and 0.8V low. The worst-case output logic levels are 2.4V high and 0.4V low. For TTL interfacing, therefore, the normal worst-case noise immunity of at least 400mV is maintained. All of the output buffers can source at least 400μA worst-case and can sink at least 3.2mA worst-case while maintaining TTL output logic levels. Other output conditions are specified to help configure non-standard interface circuitry. The logic level specifications take into account all worst-case combinations of the three variables that affect the logic level thresholds: ambient temperature, supply voltage and processing parameters. A change in any of these toward nominal values will improve the actual operating margins and will increase noise immunity.

Unprotected open gate inputs of high quality MOS transistors exhibit very high resistances on the order of perhaps 10^{14} ohms. It is easy, therefore, in some circumstances, for charge to enter the gate node of such an input faster than it can be discharged and consequently for the gate voltage to rise high enough to break down the oxides and destroy the transistor. All inputs to the Am9513 include protection networks to help prevent damaging accumulations of static charge. The protection circuitry is de-

signed to slow the transistions of incoming current surges and to provide low impedance discharge paths for voltages beyond the normal operating levels. Note, however, that input energy levels can nonetheless be too high to be successfully absorbed. Conventional design, storage, and handling precautions should be observed so that the protection networks themselves are not overstressed.

Within the limits of normal operation, the input protection circuitry is inactive and may be modeled as a lumped series RC as shown in Figure 8a. The functionally active input connection during normal operation is the gate of an MOS transistor. No active sources or drains are connected to the inputs so that neither transient nor steady-state currents are impressed on the driving signals other than the charging or discharging of the input capacitance and the accumulated leakage associated with the protection network and the input circuit. Lumped input capacitances are usually around 10pF and leakage currents are usually less than 1μA.

The only exception to the purely capacitive input case is the X2 crystal input. As shown in Figure 8b, an internal resistor connects X1 to X2 in addition to the protection network. The resistor is a modestly high value of more than 100k ohms.

Fanout from the driving circuitry into the Am9513 inputs will generally be limited by transition time considerations rather than DC current limitations when the loading is dominated by conventional MOS circuits. In an operating environment, all inputs should be terminated so they do not float and therefore will not accumulate stray static charges. Unused inputs should be tied directly to Ground or to VCC, as appropriate. An input in use will have some type of logic output driving it and termination during operation will not be a problem. Where inputs are driven from logic external to the card containing this chip, however, on-board termination should be provided to protect the chip when the board is unplugged and the input would therefore otherwise float. A pull-up resistor or a simple inverter or gate will suffice.

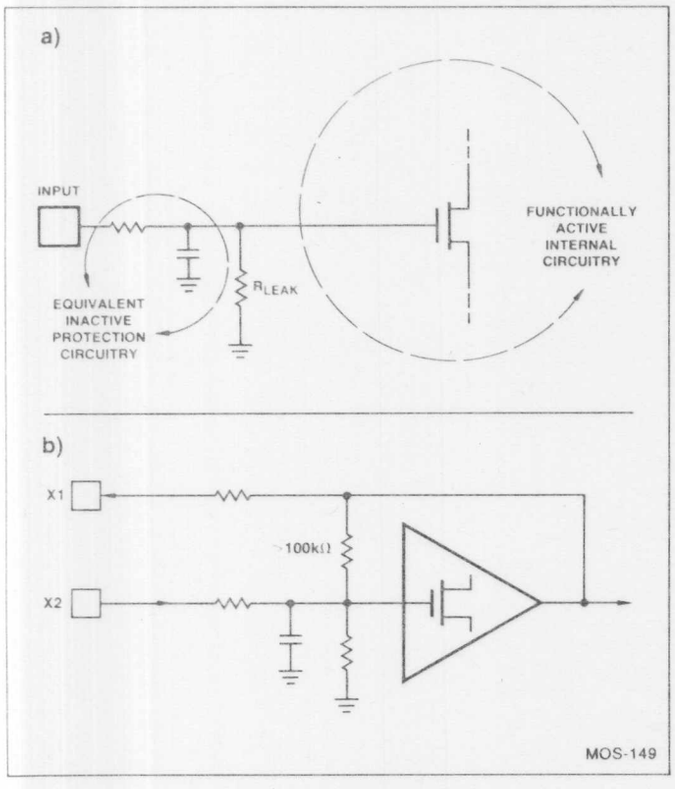


Figure 8. Input Circuitry.

Power Supply

The Am9513 requires only a single +5V power supply. The commercial temperature range parts have a voltage tolerance of ±5%; the military temperature range tolerance is ±10%. Maximum supply currents are specified in the data sheet at the high end of the voltage tolerance and the low end of the temperature range. In addition, the current specifications take into account the worst-case distribution of processing parameters that may be encountered during the manufacturing life of the product. Typical supply current values, on the other hand, are specified at a nominal +5.0 volts, a nominal ambient temperature of 25°C, and nominal processing parameters. Supply current always decreases with increasing ambient temperature; thermal run-away is not a problem.

Supply current will vary somewhat from part to part, but a given unit at a given operating temperature will exhibit a nearly constant power drain. There is no functional operating region that will cause more than a few percent change in the supply current. Decoupling of VCC, then, is straightforward and will generally be used to isolate the Am9513 from VCC noise originating externally.

CONTROL ELEMENTS

There are many addressable internal control elements, including comparators, registers and counters, within the Am9513 and they are summarized in Figure 9. The total is 444 bits that are available for control and operation of the STC. It is the unusual level of control over these elements that provides the operating versatility and much of the application diversity of the STC. Most of the registers can be both written into and read out by the host processor.

Name	Bit Size	Quantity
Output Control Bit	1	5
FOUT Divider Counter	4	1
Data Pointer Counter	6	1
Status Register	6	1
Command Register	8	1
Frequency Scaling Counter	16	1
Master Mode Register	16	1
Alarm Register	16	2
Comparator	16	2
Counter Mode Register	16	5
Counter Load Register	16	5
Counter Hold Register	16	5
General Counter	16	5

Figure 9. Control Element Summary.

Command Register

The 8-bit write-only Command register provides direct host processor software control over many general counter functions. It also provides control over the Data Pointer counter used to access the internal control elements, and allows direct manipulation of three of the Master Mode register bits. The command register is accessed by writing into the control port (see Figure 7). The "Command Description" section of this note explains the detailed operation of each command. Figure 19 summarizes the available commands.

Status Register

The 8-bit read-only Status register indicates the state of the Byte Pointer bit in the Data Pointer register and the state of the OUT

signal for each of the general counters. See Figure 10. The OUT signals reported are those internal to the chip just before the three-state interface buffer circuitry. Thus, the Status register reflects the results of polarity control over the OUT signals, and continues to indicate the counter condition even when the output is off. The Status register is normally accessed via the control port (see Figure 7) but may also be read as part of the Control Group via the data port. The "Command Description" section of this note describes this alternative Status access.

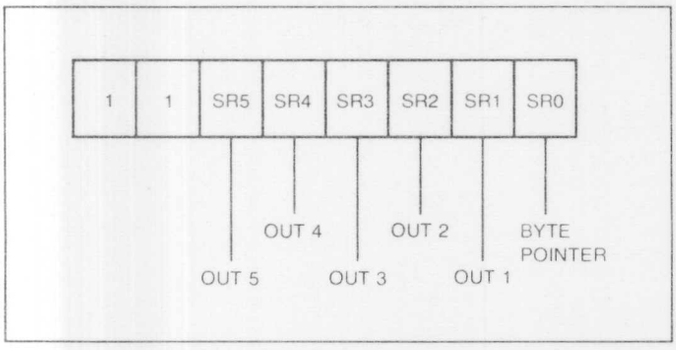


Figure 10. Status Register Bit Assignments.

Master Mode Register

The 16-bit Master Mode register (MM) is used to control the additional programmable functions that supplement the counter-specific options controlled by the individual Counter Mode registers. The "Master Mode Control Options" section of this note describes the detailed functions associated with the register. Figure 13 shows the bit assignments for the Master Mode register.

Frequency Scaler

A 16-bit scaling counter divides the output of the on-chip oscillator into four additional sub-frequencies. This provides a total of five internal frequencies that may be routed to any of the general counters and to the FOUT divider. The scaler is tapped every 4 bits and may be programmed to divide in binary or in BCD. The combinations of frequencies thus available are shown in Figure 11. For example, if the base oscillator frequency is 5MHz, then the F4 frequency will be 5kHz when BCD scaling is selected. If the base oscillator frequency is 2.4576MHz, then the F3 frequency will be 9600 Hz when binary scaling is selected. The control bit that selects BCD or binary scaling is located in the Master Mode register.

FOUT Divider

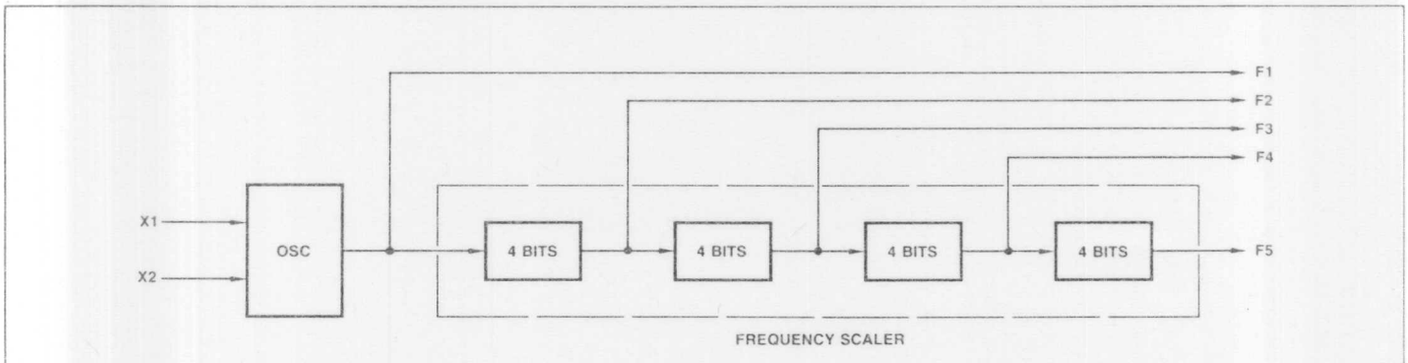
The 4-bit FOUT Divider is used to subdivide the source selected for the Frequency Out pin. It provides for division by an integer from 1 to 16, inclusive. The dividing ratio is selected by a 4-bit field in the Master Mode register. The FOUT Divider is intended to allow a relatively low FOUT frequency for use as a system clock while still permitting higher resolution internal frequencies from the crystal oscillator. With a crystal frequency of 8MHz, for example, a divider ratio of four with F1 selected would provide an FOUT rate of 2MHz. In applications that do not use FOUT as a frequency source or as a clock, the Divider forms a simple general-purpose programmable 4-bit divider that can use any of the general input pins.

Data Pointer Counter

The 6-bit Data Pointer is used to control internal addressing for data bus transfers via the data port. The Data Pointer is directly loaded by command and may be automatically incremented following data transfers. Figure 12 shows the pointer configuration.

The Byte Pointer bit is only active when the data bus is operating with its 8-bit width option. Whenever the Data Pointer is loaded, the Byte Pointer bit is set to a one. The Byte Pointer toggles following each 8-bit data transfer with an 8-bit data bus (MM13 = 0), or it always remains set with the 16-bit data bus option (MM13 = 1).

The Element Pointer field definitions vary depending on the state of the Group Pointer. When one of the Counter Groups is specified, the Element field selects one of the three 16-bit registers within the group for access. The Element Pointer also selects a type of sequencing that may be used.



Frequency	BCD Scaling MM15 = 1	Binary Scaling MM15 = 0
F1	OSC	OSC
F2	F1 ÷ 10	F1 ÷ 16
F3	F1 ÷ 100	F1 ÷ 256
F4	F1 ÷ 1,000	F1 ÷ 4,096
F5	F1 ÷ 10,000	F1 ÷ 65,536

MOS-150

Figure 11. Frequency Scaler Ratios.

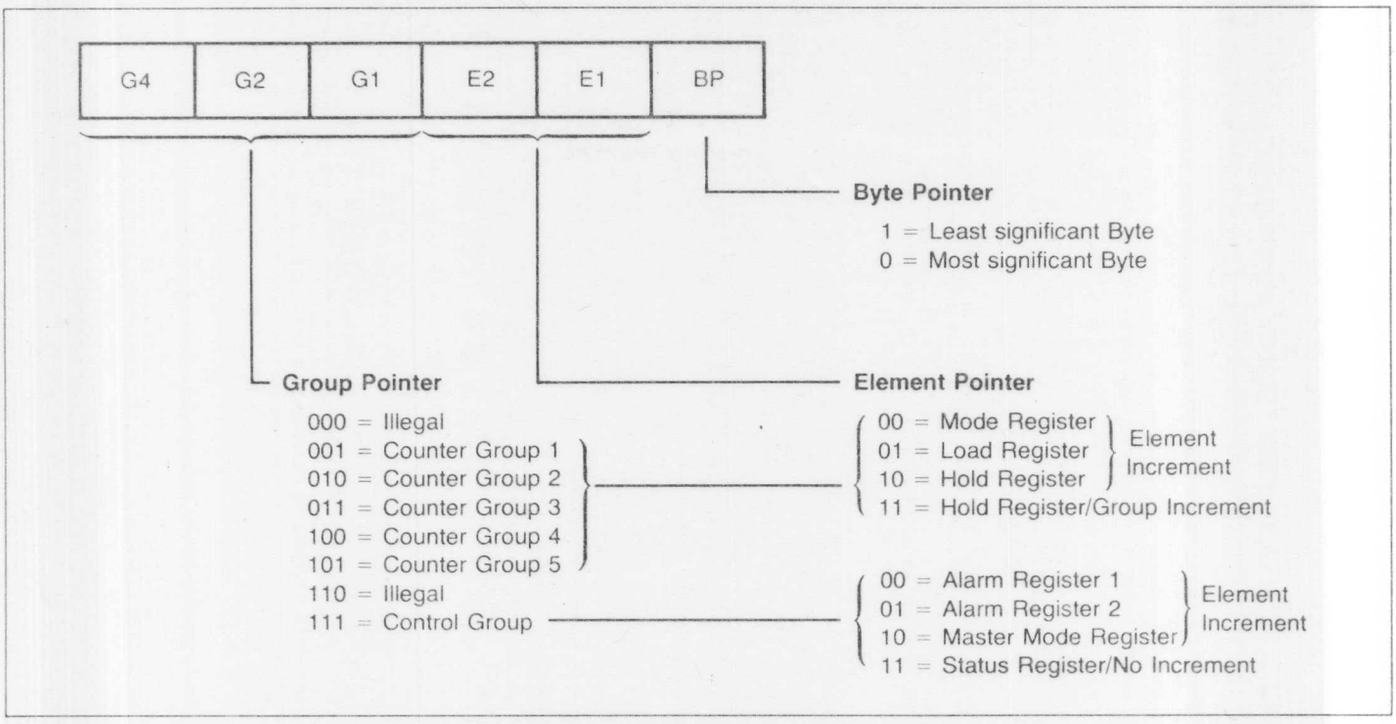


Figure 12. Data Pointer Counter.

When control bit MM14 = 1, automatic sequencing of the Data Pointer register is disabled and the contents of the Group and Element fields will change only when the Data Pointer is loaded by command. This allows the host processor to repetitively access any given internal data register without intervening commands.

When control bit MM14 = 0, the Data Pointer will automatically sequence through new pointer values as information is transferred into or out of the data port. Several types of sequencing operations are available depending on the data bus width being used and the initial Data Pointer value entered by command. When E1 = 0 or E2 = 0, and MM14 = 0, then the Element field will automatically sequence through three values: 00, 01 and 10. When the transition from 10 to 00 occurs, the Group Field will also be incremented by one. Note that the Element field in this case does not sequence to a value of 11. When E1 = 1 and E2 = 1, then only the Group field is sequenced. This allows the Hold registers to be sequentially accessed while bypassing the Mode and Load registers.

No automatic sequencing will change the Group Pointer to an illegal value.

The illegal codes may occur following power-up and the Data Pointer should always be loaded with some appropriate value during initialization.

When the Control Group is specified (G4, G2, G1 = 111), automatic increment of the Group field is disabled and the Element field will circulate through the first three values (assuming MM14 = 0). When one of the Counter Groups is specified, the G field may increment through the five Counter Group values; it will not sequence into the illegal codes or into the Control Group.

Counter Logic Groups

As shown in Figures 2 and 3, each of the five Counter Logic Groups consists of a 16-bit general counter with associated control and output logic, a 16-bit Load register, a 16-bit Hold register and a 16-bit Mode register. In addition, Counter Groups 1 and 2 also include 16-bit comparators and 16-bit Alarm registers. The comparator/alarm functions are controlled by the Master Mode register. The operation of the Counter Mode registers, then, is the same for all five counters. The host CPU has both read and write access to all registers in the Counter Logic Groups. The counter itself is never directly accessed.

Load Register

The 16-bit read/write Load register is used to control the effective length of the general counter. Any 16-bit value may be written into the Load register. That value can then be transferred into the counter each time the Terminal Count (TC) occurs. "Terminal Count" is defined as that period of time when the counter contents would have been zero if an external value had not been transferred into the counter. Thus, the terminal count frequency can be the input frequency divided by the value in the Load register. In all operating modes either Load or Hold will be transferred into the counter when TC occurs. In cases where values are being accumulated in the counter, the Load register action can become transparent by filling the Load register with all zeros.

Hold Register

The 16-bit read/write Hold register is dual-purpose. It can be used in the same way as the Load register, thus offering an alternate source for modulo definition for the counter. The Hold register may also be used to store accumulated counter values for later transfer to the host processor. This allows the count to be sampled while the counting process proceeds without interruption. Transfer of the counter contents into the Hold register is accomplished by the hardware interface in some operating modes or by software commands at any time.

Counter Mode Register

The 16-bit read/write Counter Mode register controls the gating, counting, output and source select functions within each Counter Logic Group. The "Counter Mode Control Options" section of this note describes the detailed control options available. Figure 15 shows the bit assignments for the Counter Mode registers.

Alarm Registers and Comparators

Added functions are available in the Counter Logic Groups for counters 1 and 2 (see Figure 3). Each contains a 16-bit Alarm register and a 16-bit Comparator. When the value in the counter reaches the value in the Alarm register, the Comparator output will go true. The Master Mode register contains control bits to individually enable/disable the comparators. When enabled, the comparator output appears on the OUT pin of the associated counter in place of the normal counter output. The output will remain true as long as the comparison is true, that is, until the next input causes the count to change. The Comparator output is subject to the same polarity control logic as the counter out.

In some applications, values are being accumulated and recognition of a particular count event is desired. This might be accomplished by pre-loading the counter with the desired value and then counting it down toward zero. Alternatively, the counter can be initialized with zero and the desired value entered into the Alarm register. With the Comparator enabled, an OUT transition will then occur when the value is reached, plus counts will continue to accumulate.

Output Toggle

The output control circuitry for each of the five counter groups includes a toggle flip-flop that may be used to generate various output waveforms. TC from the counter is the toggling signal and the output frequency can thus be half the TC frequency. The toggle can be initialized to either high or low state by command. More discussion of the toggle activity is included in the "Counter Mode Control Options" section of this note.

MASTER MODE CONTROL OPTIONS

The 16-bit Master Mode (MM) register is used to control those internal activities that are not controlled by the individual Counter Mode registers. This includes frequency control, time-of-day operation, comparator controls, data bus width and data pointer sequencing. Figure 13 shows the bit assignments for the Master Mode register. This section describes the use of each control field.

After power-on reset or a Master Reset command, the Master Mode register is cleared to an all zero condition. This results in the following configuration:

Time-of-day disabled
Both Comparators disabled
FOUT Source is frequency F1
FOUT Divider set for divide-by-16
FOUT gated on
Data Bus 8 bits wide
Data Pointer Sequencing enabled
Frequency Scaler divides in binary

Time-of-Day

Bits MM0 and MM1 of the Master Mode register specify the time-of-day (TOD) options. When MM0 = 0 and MM1 = 0 the special logic used to implement TOD is disabled and counters 1 and 2 will operate in exactly the same ways as counters 3, 4 and

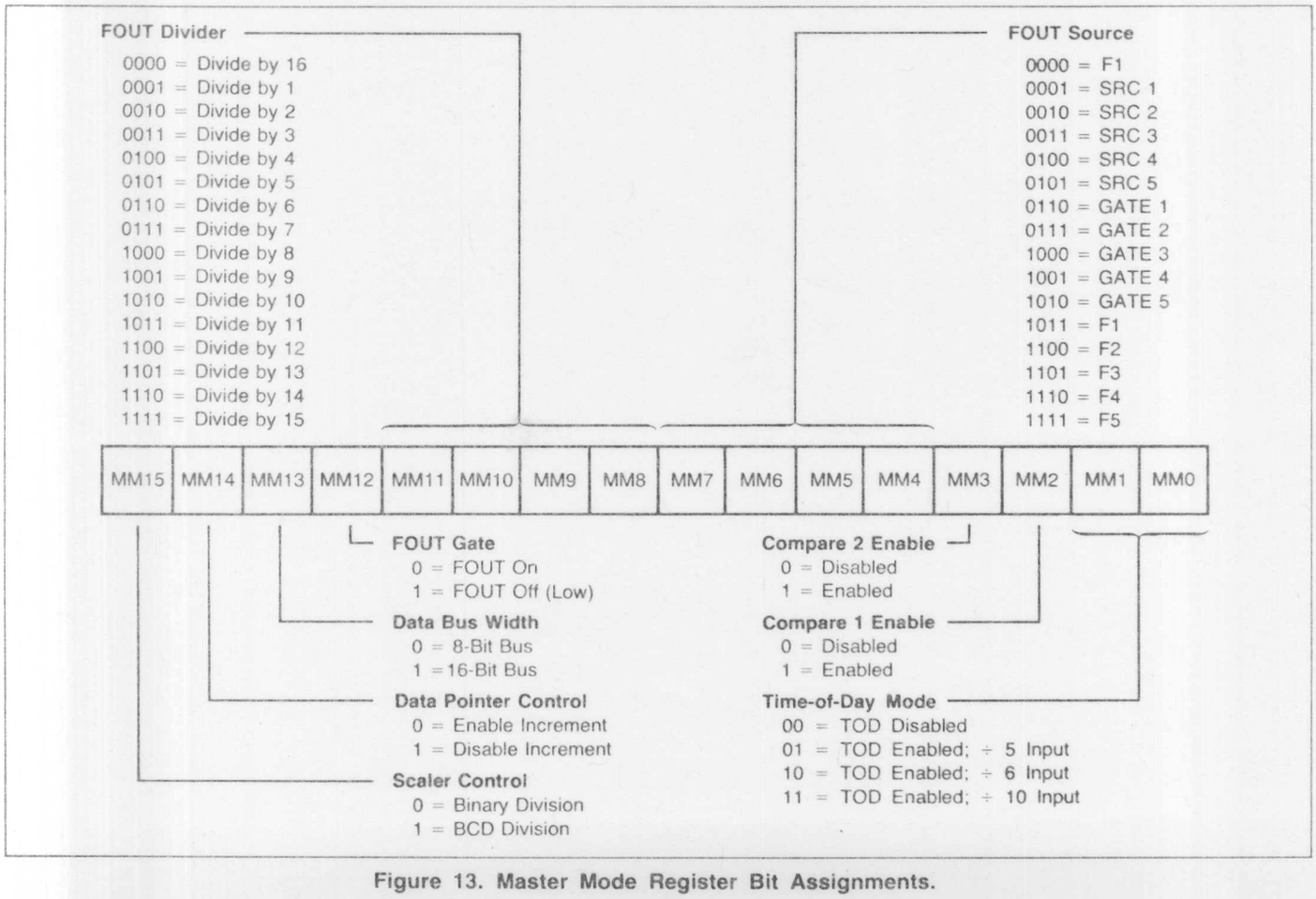


Figure 13. Master Mode Register Bit Assignments.

5. When MM0 = 1 or MM1 = 1, additional counter decoding and control logic is enabled on counters 1 and 2 which causes them to turn-over at the counts that generate appropriate 24-hour TOD accumulations.

Figure 14 shows the counter configurations for TOD operation. The two most significant decades of Counter 2 contain the "hours" digits and they can hold a maximum count of 23 hours. The two least significant decades of Counter 2 indicate "minutes" and will hold values up to 59. The three most significant decades of Counter 1 indicate "seconds" and will contain values up to 59.9. The least significant decade of Counter 1 is used to scale the input frequency in order to output tenth-of-second periods into the next decade. It can be set up to divide by five (MM0 = 1, MM1 = 0), divide by six (MM0 = 0, MM1 = 1), or divide by ten (MM0 = 1, MM1 = 1). The input frequency, therefore, for realtime clocking can be, respectively, 50Hz, 60Hz or 100Hz. With divide-by-ten specified and with 100Hz input, the least significant decade of Counter 1 accumulates time in hundredths of seconds (tens of milliseconds). For accelerated time applications other input frequencies may be useful.

The input for Counter 2 should be the output of Counter 1, connected either internally or externally, for TOD operation. Both counters should be set up for BCD counting. The Load registers should be used to initialize the counters to the proper time and then should be filled with zeros. Either count up or count down may be used.

Comparator Enable

Bits MM2 and MM3 control the Comparators associated with Counters 1 and 2. When a Comparator is enabled its output is substituted for the normal counter output on the associated OUT1 or OUT2 pin. The polarity definition for the comparator output will depend on the active-high or active-low definition as programmed in the appropriate Counter Mode register. Once the compare output is true, it will remain so until the count changes and the comparison therefore goes false.

The two Comparators can always be used individually in any operating mode. One special case occurs when the time-of-day option is invoked and both Comparators are enabled. The operation of Comparator 2 will then be conditioned by Comparator 1 so that a full 32-bit compare must be true in order to generate a true signal on OUT2. OUT1 will continue, as usual, to reflect the state of the 16-bit comparison between Alarm 1 and Counter 1.

FOUT Source

Master Mode bits MM4 through MM7 specify the source input for the FOUT Divider. 15 inputs are available for selection and they include the five Source pins, the five Gate pins and the five internal frequencies derived from the oscillator. The 16th combination of the four control bits (all zeros) is used to assure that an active frequency is available on FOUT following reset.

FOUT Divider

Bits MM8 through MM11 specify the dividing ratio for the FOUT Divider. The FOUT source selected by bits MM4 through MM7 is divided by an integer value between 1 and 16, inclusive, and is then passed to the FOUT output buffer. The undivided Oscillator frequency is available at FOUT simply by selecting the F1 source and a dividing ratio of one. After power-on or reset, the FOUT Divider is set to divide by sixteen.

FOUT Gate

Master Mode bit MM12 provides a software gating capability for the FOUT signal. When MM12 = 1, FOUT is off and in a low impedance state to ground. MM12 may be set or cleared in conjunction with the loading of the other bits in the Master Mode register; alternatively, there are commands that allow MM12 to be individually set or cleared directly without changing any other Master Mode bits. After power-up or reset, FOUT is gated on.

Bus Width

Bit MM13 controls the multiplexer at the data bus interface in order to configure the part for an 8-bit or 16-bit external bus. The internal bus is always 16-bits wide. When MM13 = 1, 16-bit data is transferred directly between the internal bus and all 16 of the external bus lines. In this configuration the Byte Pointer bit (in the Data Pointer register) remains reset at all times. When MM13 = 0, 16-bit internal data is transferred a byte at a time to and from the eight low-order external data bus lines. The Byte Pointer bit toggles with each byte transfer in this mode.

Data Pointer Sequencing

Bit MM14 controls the Data Pointer logic to enable or disable the automatic sequencing functions. When MM14 = 1, the contents of the Data Pointer can be changed only directly by entering a command. When MM14 = 0, several types of automatic

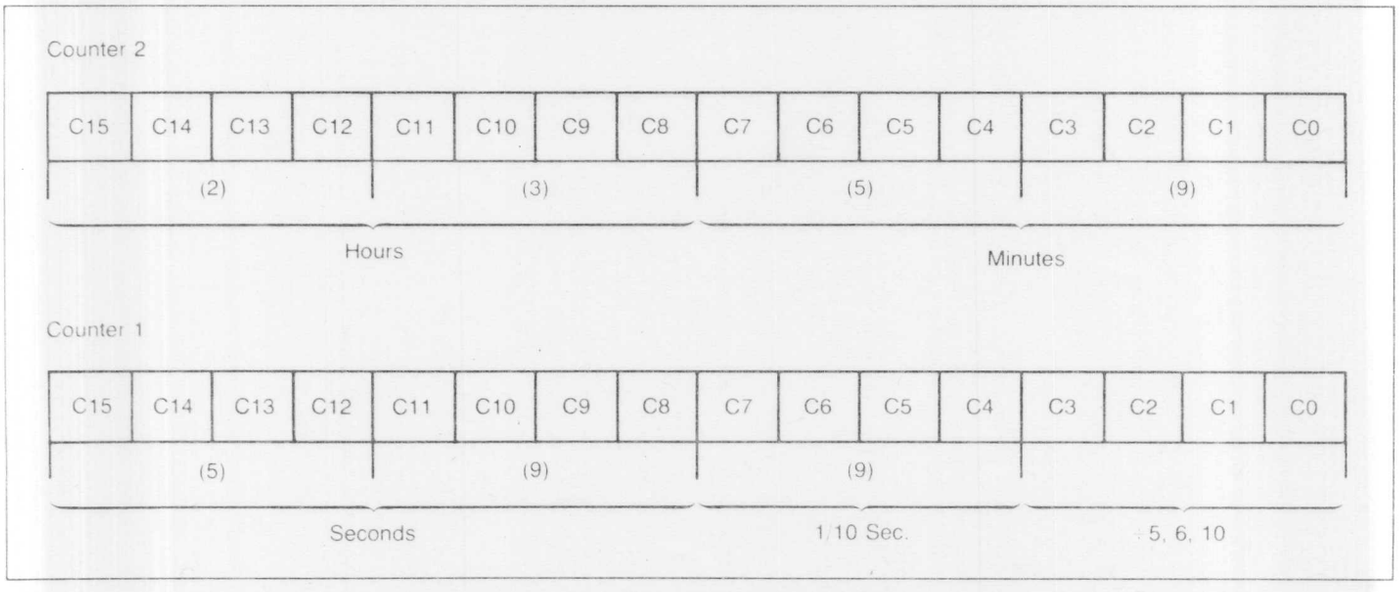


Figure 14. Time-of-Day Configuration.

sequencing of the Data Pointer are available. Thus the host processor, by controlling MM14, may repetitively read/write a single internal location, or may sequentially read/write groups of locations.

Scaler Ratios

Master Mode bit MM15 controls the counting configuration of the Frequency Scaler counter. When MM15 = 0, the Scaler divides the oscillator frequency in binary steps so that each sub-frequency is 1/16 of the preceding frequency. When MM15 = 1, the Scaler divides in BCD steps so that adjacent frequencies are related by ratios of 10 instead of 16. See Figure 11.

COUNTER MODE CONTROL OPTION

Each Counter Logic Group includes a Counter Mode (CM) register used to control all of the individual options available with its associated general counter. These options include output configuration, count control, count source and gating control. Figure 15 shows the bit assignments for the Count Mode registers. This section describes the control options in detail. Note that generally each counter is independently configured and does not depend on information outside its Counter Logic Group.

After power-on reset or a Master Reset command, the Counter Mode registers are initialized to a preset condition. The value entered is 0B00 hex and results in the following control configuration:

Output low impedance to ground
Count down
Count binary
Count once
Load register selected
No retriggering
F1 input source selected
Positive-true input polarity
No gating

Output Control

Counter Mode bits CM0 through CM2 specify the output control configuration. The OUT pin may be off and in a high impedance state, or it may be off with a low impedance to ground. The six remaining combinations are split into active-high and active-low versions of the three basic output waveforms.

One output form available is called Terminal Count (TC) and represents the period of time that the counter reaches an equivalent value of zero. Figure 16 shows a Terminal Count pulse and an example context that generated it. Notice that the TC width is determined by the period of the counting source. Figure 16 assumes active-high source polarity, counter armed, gate active, counter decrementing and a reload value of K.

The counter will always be updated when TC occurs; the user can choose the source location and the value. If a non-zero value is picked, the counter will never really attain a zero state and TC will indicate the counter state that would have been zero had no parallel transfer occurred.

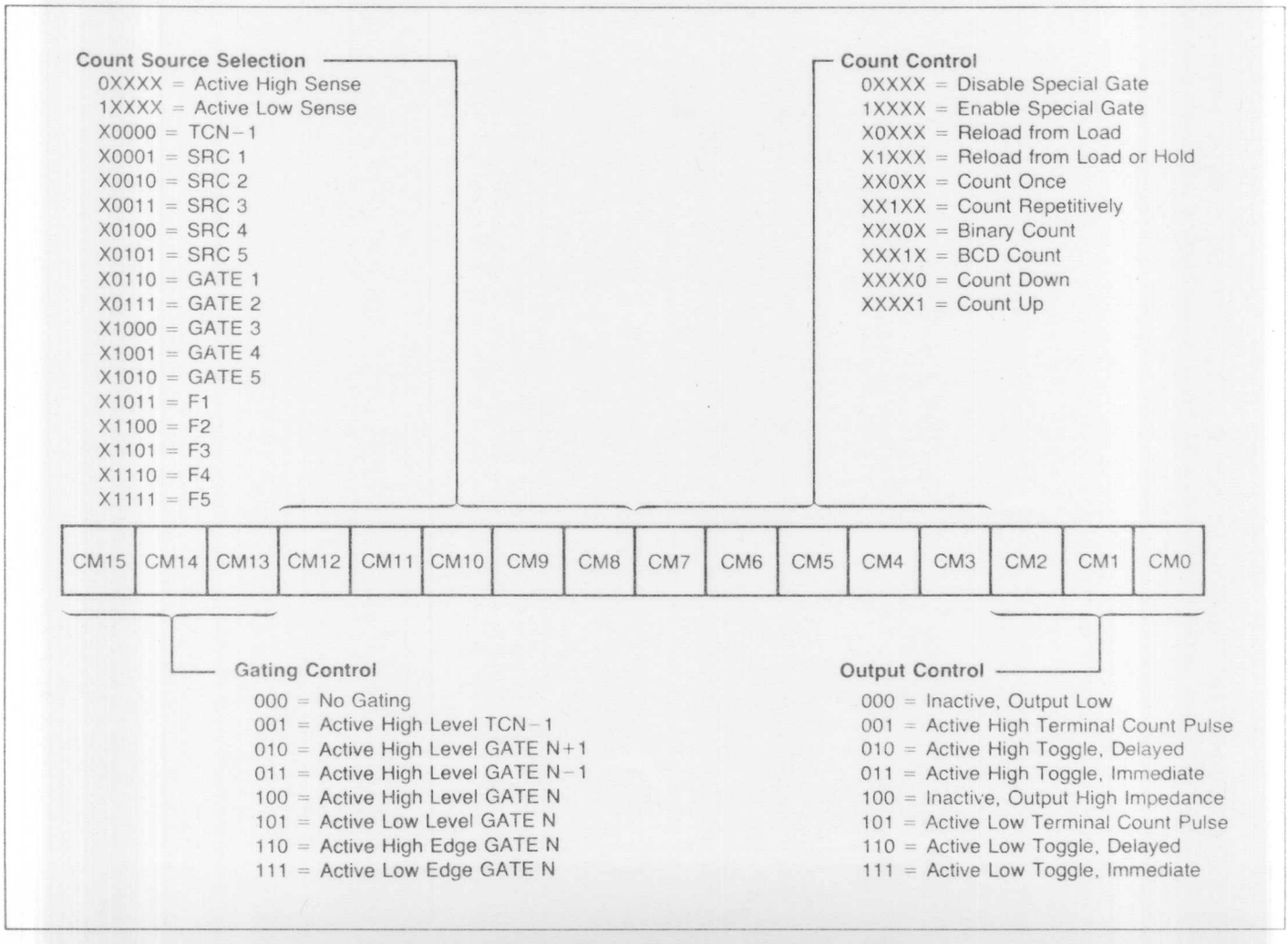


Figure 15. Counter Mode Register Bit Assignments.

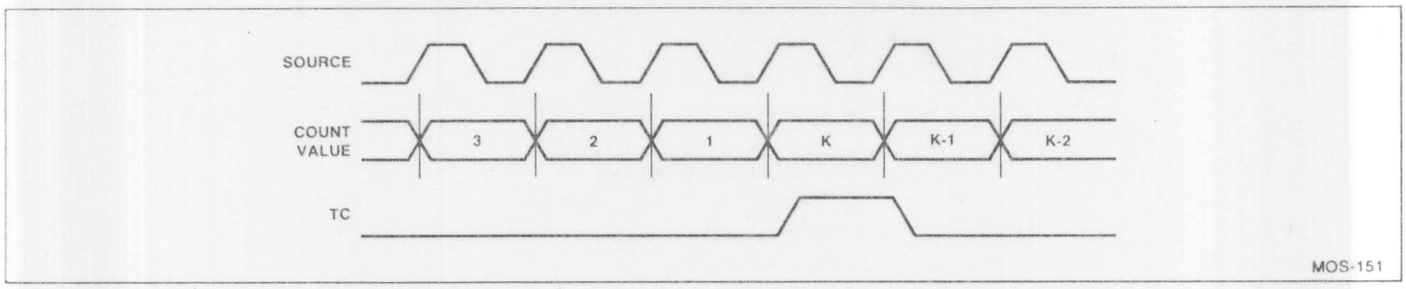


Figure 16. TC Waveform Format.

Another output form uses the output control toggle to generate an output level instead of a pulse. Two variations of the toggle waveforms are available, as shown in Figure 17. The one labeled "Delayed" uses only the TC pulse to trigger the toggle; since TC does not occur until a full count elapses following the arming of the counter, the first transition of the toggle is delayed from the moment of arming. On the other hand, the waveform labeled "Immediate" also uses the TC pulse as the toggling source but adds a toggle transition on the first count following the arming. After the initial transition, both Delayed and Immediate waveforms are the same; for the same output polarity they will be 180° out of phase. The trailing edge of TC triggers the toggle. The toggle waveforms are half the frequency of TC.

Count Control

Counter Mode bits CM3 through CM7 specify the various options available for direct control of the counting process. Most of the control bits operate relatively independently of the others so that they may be combined freely to form many types of counting configurations.

Bit CM3 specifies incrementing or decrementing of the counter. For many timing and frequency division purposes, down-counting is preferred since the key value is identified when the counter reaches zero. Alternatively, for event counting or elapsed time applications, up-counting will be preferred so that accumulated values can be conveniently handled. CM3 may be changed during a counting process in order to generate special functions.

Bit CM4 selects binary or BCD counting. This option greatly simplifies the interface with the host system by helping to minimize format conversions. Indeed, this capability can be used in some cases to make conversions.

Bit CM5 controls the repetition of the count process. When CM5 = 1, counting will proceed in the specified mode until the counter is disarmed or the mode is changed. When CM5 = 0, the count process will proceed only until one or two TC events occur. The counter is then disarmed automatically. The single or double TC requirement will depend on the state of other control bits.

When TC occurs, the counter is always reloaded with a value from either the Load register or the Hold register. Bit CM6 specifies the source options for reloading the counter. When CM6 = 0 the contents of the Load register will be transferred into the counter at every occurrence of TC and when CM6 = 1 the counter reload location will be either the Load or Hold Register. These locations can alternate or can be controlled by a GATE pin. With alternating sources and with the toggle output selected, the duty cycle of the output waveform is controlled by the relative Load and Hold values and very fine resolution of duty cycle ratios will then be available in many circumstances.

Bit CM7 controls the special gating functions that allow retriggering and the selection of Load or Hold sources for counter reloading. The use and definition of CM7 will depend on the status of the Gating Control field and bits CM5 and CM6.

When some form of Gating is specified, CM7 controls hardware retriggering. In this case, when CM7 = 0 hardware retriggering does not occur; when CM7 = 1 the counter is reloaded any time an active Gate input occurs. Any time that retriggering occurs, the Counter contents are transferred into the Hold register. When No Gating is specified, the definition of CM7 changes. In this case, when CM7 = 0 the Gate input has no effect on the counting; when CM7 = 1 the Gate input specifies the source used to reload the counter when TC occurs. Figure 18 shows the various available control combinations for these interrelated bits.

Count Source Selection

Counter Mode bits CM8 through CM12 specify the source used as input to the counter and the active edge that is counted. Bit CM12 controls the polarity for all the sources with logic zero indicating active high and logic one indicating active low. Bits CM8 through CM11 select one of sixteen counting sources to route to the counter input. Five of the available inputs are internal frequencies derived from the internal oscillator. (See Figure 11 for frequency assignments.) Ten of the available inputs are interface pins; five are labeled SRC and five are labeled GATE.

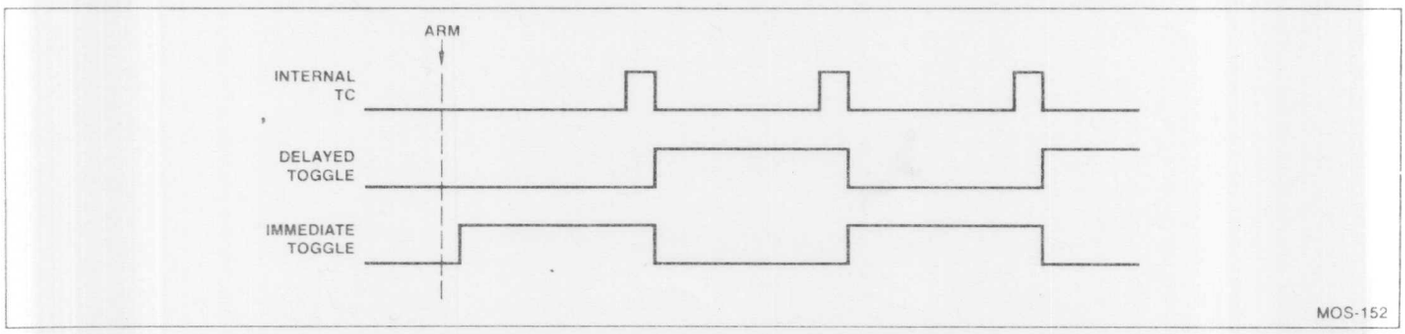


Figure 17. Output Waveform Format.

Operating Mode	A	B	C	D	E	F	G	H	I	J	K	L
Special Gate (CM7)	0	0	0	0	0	0	0	0	0	0	0	0
Reload Source (CM6)	0	0	0	0	0	0	1	1	1	1	1	1
Repetition (CM5)	0	0	0	1	1	1	0	0	0	1	1	1
Gate Control (CM15-CM13)	000	LEVEL	EDGE	000	LEVEL	EDGE	000	LEVEL	EDGE	000	LEVEL	EDGE
Count to TC once, then disarm	X	X	X									
Count to TC twice, then disarm							X	X	X			
Count to TC repeatedly				X	X	X				X	X	X
Gate input does not gate counter input	X			X			X			X		
Count only during active gate level		X			X			X			X	
Start count on active gate edge and stop count on next TC.			X			X						
Start count on active gate edge and stop count on second TC.									X			X
No hardware retriggering	X	X	X	X	X	X	X	X	X	X	X	X
Reload counter from Load Register on TC	X	X	X	X	X	X						
Reload counter on each TC, alternating reload source between Load and Hold Registers.							X	X	X	X	X	X
Transfer Load Register into counter on each TC that gate is LOW; transfer Hold Register into counter on each TC that gate is HIGH.												
On active gate edge transfer counter into Hold Register and then reload counter from Load Register.												
On active gate edge transfer counter into Hold Register and then reload counter from Load or Hold Register.												

Operating Mode	M	N	O	P	Q	R	S	T	U	V	W	X
Special Gate (CM7)	1	1	1	1	1	1	1	1	1	1	1	1
Reload Source (CM6)	0	0	0	0	0	0	1	1	1	1	1	1
Repetition (CM5)	0	0	0	1	1	1	0	0	0	1	1	1
Gate Control (CM15-CM13)	000	LEVEL	EDGE	000	LEVEL	EDGE	000	LEVEL	EDGE	000	LEVEL	EDGE
Count to TC once, then disarm		X	X									
Count to TC twice, then disarm							X	X	X			
Count to TC repeatedly					X	X				X	X	X
Gate input does not gate counter input							X			X		
Count only during active gate level		X			X			X			X	
Start count on active gate edge and stop count on next TC.			X			X						
Start count on active gate edge and stop count on second TC.									X			X
No hardware retriggering							X			X		
Reload counter from Load Register on TC		X	X		X	X						
Reload counter on each TC, alternating reload source between Load and Hold Registers.								X	X		X	X
Transfer Load Register into counter on each TC that gate is LOW; transfer Hold Register into counter on each TC that gate is HIGH.							X			X		
On active gate edge transfer counter into Hold Register and then reload counter from Load Register.		X	X		X	X						
On active gate edge transfer counter into Hold Register and then reload counter from Load or Hold Register.								X	X		X	X

Note: Operating modes M and P should not be used.

Figure 18. Counter Control Interaction.

The sixteenth available input is the TC output from the adjacent lower-numbered counter. (The Counter 5 TC wraps around to the Counter 1 input.) This option allows internal concatenating that permits very long counts to be accumulated. Since all five counters may be concatenated, it is possible to configure a counter that is 80 bits long on one Am9513 chip. When TCN−1 is the source, the count ripples between the connected counters. External connections can also be made, and can use the toggle bit for even longer counts. This is easily accomplished by selecting a TOG output mode and wiring OUTN to one of the SRC inputs.

Gating Control

Counter Mode bits CM13 through CM15 specify the hardware gating options. When "no gating" is selected (000) the counter will proceed unconditionally as long as it is armed. For any other gating mode, the count process is conditioned by the specified gating configuration.

For a code of 100 in this field, counting can proceed only when the pin labeled GATEN associated with Counter N is at a logic high level. When it goes low, counting is simply suspended until the Gate goes high again. A code of 101 performs the same function with an opposite active polarity. Codes 010 and 011 offer the same function as 100, but specify alternate input pins as Gating Sources. This allows any of three interface pins to be used as gates for a given counter. On Counter 4, for example, pin 34, pin 35 or pin 36 may be used to perform the gating function. This also allows a single Gate pin to simultaneously control up to three counters.

For codes of 110 or 111 in this field, counting proceeds after the specified active Gate edge until one or two TC events occur. Within this interval the Gate input is ignored, except for the retriggering option. When repetition is selected, a cycle will be repeated as soon as another Gate edge occurs. This mode is useful when implementing a digital single-shot since the gate can serve as a convenient firing trigger.

A 001 code in this field selects the TC output from the adjacent lower-numbered counter as the gate. Thus, one counter may be configured to generate a counting "window" for another counter.

COMMAND DESCRIPTIONS

The command set for the Am9513 allows the host processor to customize and manage the operating modes and features for particular applications, to initialize and update both the internal data and control information, and to manipulate operating bits during operation. Commands are entered directly into the 8-bit Command register by writing into the Control port (see Figure 7).

All available commands are described in the following text. Figure 19 summarizes the command codes and includes a brief description of each function. Figure 20 shows all the unused code combinations; unused codes should not be entered into the Command register since undefined activities may occur.

Six of the command types are used for direct software control of the counting process and they each contain a five-bit S field. In a linear-select fashion, each bit in the S field corresponds to one of the five general counters (S1 = Counter 1, S2 = Counter 2, etc.). When an S bit is a one, the specified operation is performed on the counter so designated; when an S bit is a zero, no operation occurs for the corresponding counter. This type of command format has three basic advantages. It saves host software by allowing any combination of counters to be acted on by a single command. It allows simultaneous action on multiple counters where synchronization of commands is important. It allows

Command Code								Command Description
C7	C6	C5	C4	C3	C2	C1	C0	
0	0	0	E2	E1	G4	G2	G1	Load Data Pointer register with contents of E and G fields. (G ≠ 000, G ≠ 110)
0	0	1	S5	S4	S3	S2	S1	Arm counting for all selected counters
0	1	0	S5	S4	S3	S2	S1	Load contents of specified source into all selected counters
0	1	1	S5	S4	S3	S2	S1	Load and Arm all selected counters
1	0	0	S5	S4	S3	S2	S1	Disarm and Save all selected counters
1	0	1	S5	S4	S3	S2	S1	Save all selected counters in hold register
1	1	0	S5	S4	S3	S2	S1	Disarm all selected counters
1	1	1	0	1	N4	N2	N1	Set output bit N (001 ≤ N ≤ 101)
1	1	1	0	0	N4	N2	N1	Clear output bit N (001 ≤ N ≤ 101)
1	1	1	1	0	N4	N2	N1	Step counter N (001 ≤ N ≤ 101)
1	1	1	0	1	0	0	0	Set MM14 (Disable Data Pointer Sequencing)
1	1	1	0	1	1	1	0	Set MM12 (Gate off FOUT)
1	1	1	0	1	1	1	1	Set MM13 (Enter 16-bit bus mode)
1	1	1	0	0	0	0	0	Clear MM14 (Enable Data Pointer Sequencing)
1	1	1	0	0	1	1	0	Clear MM12 (Gate on FOUT)
1	1	1	0	0	1	1	1	Clear MM13 (Enter 8-bit bus mode)
1	1	1	1	1	1	1	1	Master reset

Figure 19. Am9513 Command Summary.

counter-specific service routines to control individual counters without needing to be aware of the operating context of other counters.

C7	C6	C5	C4	C3	C2	C1	C0
1	1	1	1	0	0	0	0
1	1	1	1	0	1	1	0
1	1	1	1	0	1	1	1
0	0	0	X	X	1	1	0
0	0	0	X	X	0	0	0
* 1	1	1	1	1	X	X	X

*Unused except when XXX = 111

Figure 20. Am9513 Unused Command Codes.

Arm Counters

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
0	0	1	S5	S4	S3	S2	S1

Description: Any combination of counters, as specified by the S field, will be enabled for counting. A counter must be armed before counting can commence. Once armed, the counting process may be further enabled or disabled using the hardware gating facilities. The ARM and DISARM commands permit software gating of the count process, where desired. This command can only arm or do nothing for a given counter; a zero in the S field does not disarm the counter.

Load Counters

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
0	1	0	S5	S4	S3	S2	S1

Description: Any combination of counters, as specified in the S field, will be loaded with previously entered values. The source of information for each counter will be either the associated Load register or the associated Hold register, as determined by the operating configuration in the Mode register. The Load/Hold contents are not changed. This command will cause a transfer independent of any current operating configuration for the counter. It will often be used as a software retrigger, or as counter initialization prior to active hardware gating.

Load and Arm Counters

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
0	1	1	S5	S4	S3	S2	S1

Description: Any combination of counters, as specified in the S field, will be first loaded and then armed. This command combines the effects of the separate ARM command and LOAD command.

Disarm Counters

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
1	1	0	S5	S4	S3	S2	S1

Description: Any combination of counters, as specified by the S field, will be disabled from counting. A disarmed counter will cease all counting independent of other control condtions. A disarmed counter may be updated using the LOAD command and may be read using the SAVE command. A count process may be resumed using an ARM command.

Save Counters

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
1	0	1	S5	S4	S3	S2	S1

Description: Any combination of counters, as specified by the S field, will have their contents transferred into their associated Hold register. The transfer takes place without interfering with any counting that may be underway. This command will overwrite any previous Hold register contents. The SAVE command is designed to allow an accumulated count to be preserved so that it can be read by the host CPU at some later time.

Disarm and Save Counters

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
1	0	0	S5	S4	S3	S2	S1

Description: Any combination of counters, as specified by the S field, will be first disarmed and then the contents transferred into the associated Hold registers. This command combines the effects of the separate DISARM command and SAVE command.

Set Output

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
1	1	1	0	1	N4	N2	N1

$(001 \leq N \leq 101)$

Description: The output toggle for counter N is set. The OUTN signal will be driven high or low depending on the output polarity configuration, unless TC out is specified.

Clear Output

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
1	1	1	0	0	N4	N2	N1

$(001 \leq N \leq 101)$

Description: The output toggle for counter N is reset. The OUTN signal will be driven high or low depending on the output polarity configuration, unless TC out is specified.

Step Counter

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
1	1	1	1	0	N4	N2	N1

$(001 \leq N \leq 101)$

Description: Counter N is incremented or decremented by one, depending on its operating configuration. If the Counter Mode register associated with the selected counter has its CM3 bit cleared to zero, this command will cause the counter to decrement by one. If CM3 is set to a logic high, this command will

increment the counter by one. The STEP command will take effect even on a disarmed counter.

Disable Data Pointer Sequencing

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
1	1	1	0	1	0	0	0

Description: This command sets Master Mode bit 14 without affecting other bits in the Master Mode register. MM14 controls the automatic sequencing of the Data Pointer register. Disabling the sequencing allows repetitive host processor access to a given internal location without repetitive updating of the Data Pointer. MM14 may also be controlled by loading a full word into the Master Mode register.

Enable Data Pointer Sequencing

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
1	1	1	0	0	0	0	0

Description: This command clears Master Mode bit 14 without affecting other bits in the Master Mode register. MM14 controls the automatic sequencing of the Data Pointer register. Enabling the sequencing allows sequential host processor access to several internal locations without repetitive updating of the Data Pointer. MM14 may also be controlled by loading a full word into the Master Mode register.

Enable 16-Bit Data Bus

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
1	1	1	0	1	1	1	1

Description: This command sets Master Mode bit 13 without affecting other bits in the Master Mode register. MM13 controls the multiplexer in the data bus buffer. When MM13 is set, no multiplexing takes place and all 16 external data bus lines are used to transfer information into and out of the STC. MM13 may also be controlled by loading the full Master Mode register in parallel.

Enable 8-Bit Data Bus

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
1	1	1	0	0	1	1	1

Description: This command clears Master Mode bit 13 without affecting other bits in the Master Mode register. MM13 controls the multiplexer in the data bus buffer. When MM13 is cleared, the multiplexer is enabled and 16-bit internal information is transferred eight bits at a time to the eight low-order external data bus lines. MM13 may also be controlled by loading the full Master Mode register in parallel.

Gate Off FOUT

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
1	1	1	0	1	1	1	0

Description: This command sets Master Mode bit 12 without affecting other bits in the Master Mode register. MM12 controls the output state of the FOUT signal. When gated off, the FOUT line will exhibit a low impedance to ground. MM12 may also be controlled by loading the full Master Mode register in parallel.

Gate On FOUT

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
1	1	1	0	0	1	1	0

Description: This command clears Master Mode bit 12 without affecting other bits in the Master Mode register. MM12 controls the output status of the FOUT signal. When MM12 is cleared, FOUT will become active and will drive out the selected and divided FOUT signal. MM12 may also be controlled by loading the full Master Mode register in parallel.

Load Data Pointer Register

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
0	0	0	E2	E1	G4	G2	G1

(G4, G2, G1 $\neq$ 000, $\neq$ 110)

Description: Bits in the E and G fields will be transferred into the corresponding Element and Group fields of the Data Pointer register as shown in Figure 12. The Byte Pointer bit in the Data Pointer register is cleared. Transfers into the Data Pointer only occur for G field values of 001, 010, 011, 100, 101 and 111. Values of 000 and 110 for G should not be used.

Master Reset

Coding:

C7	C6	C5	C4	C3	C2	C1	C0
1	1	1	1	1	1	1	1

Description: The Master Reset command duplicates the action of the power-on reset circuitry. It acts to disarm all registers and it enters a specific operating configuration into the Master Mode register and into all of the Counter Mode registers.

OPERATING INFORMATION

Reset

The reset function in the Am9513 is accomplished in two ways: automatically during power-up and by software Master Reset command. Power-up reset circuitry is internally triggered by the rising VCC voltage when a predetermined threshold is reached. An internal flip-flop is set by the rising supply voltage and controls the reset operation. The reset flip-flop remains set until cleared by the first active Chip Select input. A reset may also be initiated by the host processor by entering the Master Reset command. This software reset is active for the duration of the command write; otherwise it performs the same function as the power-up reset.

Following either type of reset, all five general counters are disarmed and will be initialized to count down in binary from a positive-going internal frequency source. The counter outputs will be off with a low impedance to ground. FOUT will be enabled and will supply a frequency 1/16 that of the internal oscillator. The Command register is cleared to zero, and all Load and Hold registers are cleared to zero. Reset does not affect the Data Pointer contents.

Information Transfer Protocols

The control signal configurations for all information transfers on the Am9513 data bus are summarized in Figure 7. The interface control logic assumes these conventions:

1. $\overline{RD}$ and $\overline{WR}$ are never active at the same time.
2. $\overline{RD}$, $\overline{WR}$, and C/$\overline{D}$ are ignored unless $\overline{CS}$ is low.

Transfers at the Control port (C/$\overline{D}$ = 1) allow direct access to the command register when writing and the status register when reading. All other available internal locations are accessed for both reading and writing via the data port (C/$\overline{D}$ = 0). Data transfers are executed to and from the location currently addressed by the Data Pointer register. Options available in the Master Mode register and the Data Pointer control structure allow several types of transfer sequencing to be used.

Random access to any available internal data location can be accomplished by simply loading the Data Pointer with a command and then initiating a data read or data write. This procedure can be used at any time, regardless of the Data Pointer control configuration. When the 8-bit data bus configuration is being used (MM13 = 0), two bytes of data would normally be transferred following the addressing command. Each time the Data Pointer is loaded, the Byte Pointer bit is set and points to the least significant byte of the addressed data location.

Automatic sequential access to the Load, Hold and Counter Mode registers of all five counter groups is possible. This is accomplished by enabling Data Pointer sequencing (MM14 = 0) and using an appropriate command to load the proper E and G field in the Data Pointer. Once this procedure is initiated, no additional commands are needed as long as sequential transfers are desired. Automatic sequential access to only the five Hold registers is accomplished in the same way except that a different initial command is used with E = 11. Notice that disabling the sequencing (MM14 = 1) allows repetitive transfers into or out of a location selected by an initial command, without further command intervention.

The Control Group elements (Master Mode, Alarm1 and Alarm2 registers) may be accessed sequentially when MM14 = 0 by using an appropriate initial command. The Control Group will not sequence into a Counter Group and vice versa. If the Control Group is specified with E = 11, the Status Register may be accessed and no subsequent Data Pointer sequencing takes place.

Initialization

Following power-up, many potential initialization procedures are possible. Often an appropriate sequence will depend heavily on the applications being addressed. It may be convenient to divide software management of the Am9513 into (at least) two primary types of operations. The first can be a simple initialization table that is used to load the desired operating values into all internal locations. The second category might consist simply of application-specific or counter-specific routines that dynamically monitor and modify the operating conditions and context of the STC.

A table-driven initialization routine is relatively easy to accomplish by exploiting the automatic Data Pointer sequencing capability of the Am9513. One possible approach, in a 16-bit environment, is illustrated by the following procedure (coding in Hex.) When making byte entries from a 16-bit data bus, the upper byte should be FF, as shown.

1. Enter Master Reset command (FFFF).
2. Enter command to switch into 16-bit bus operation (FFE7).
3. Enter command to initialize Data Pointer with first Counter Group address (FF01).
4. Fetch word from table of initial values and write into data port. Repeat using successive table entries until 15 words are transferred.
5. Enter command to initialize Data Pointer with first Control Group address (FF07).
6. Fetch next word from table and write into data port. Repeat using successive table entries until 3 words are transferred.
7. Transfer program control to other system initialization routines. When application program is run, ARM or LOAD-and-ARM commands will be entered to activate appropriate counters.

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